Brian Richard Tauro

Room 115 – Stuart Building
Department of computer science 10 W. 31st St Chicago

+1 (312) 687-3653 • btauro@hawk.iit.edu • HExSA Lab

My research interests include low-level system software, the intersection of OS kernels and compilers, data flow architectures, analysis of abstractions used to solve problems in large codebases, lower bound analysis of classical algorithms, modern day compiler abstractions, network security, accelerators and GPU architectures.

EDUCATION

Illinois Institute of Technology **Chicago, USA**
Ph.D. in Computer Science, *August 2019 - Present*
Advisor: Kyle C. Hale

Illinois Institute of Technology **Chicago, USA**
Master of Science in Computer Science, GPA 3.8 *August 2017 - May 2019*
Advisor: Kyle C. Hale

Karunya University **Coimbatore, India**
Bachelor in Technology in Computer Science, GPA 8.4 *July 2012 - May 2016*

WORK EXPERIENCE

Samsung **San Jose, USA**
Operating Systems/Runtime Intern *May 2023 - August 2023*

- I worked on automatic transformation of MPI HPC code to disaggregated hardware using modern compiler analysis and transformation.

Intel **Oregon, USA**
Multi Kernel Intern *May 2022 - August 2022*

- Study of interference between HPC and memory dis aggregated applications, where memory dis aggregation mechanisms are implemented in the mOS kernel.

Illinois Institute of Technology **Chicago, USA**
Research Assistant *August 2018 – Present*

- Develop CARM (Compiler assisted Remote Memory) a transparent far memory solution to improve memory utilization in data-centers using modern day compiler-framework (LLVM) analysis and transformation.
- Develop speedup models to estimate speedup in multi-kernels (used in super computers).
- Built an InfiniBand (Mellanox ConnectX-3) device driver for Nautilus (aerokernel) in C, in order to leverage the advanced features (RDMA, SR-IOV) provided by smart NIC's to enable low latency communication between applications running in kernel space in Nautilus.
- Instrument Linux to understand floating point save/restore register overheads in the kernel.
- Implement lazy floating point usage in kernel space in Nautilus (aerokernel) as Nautilus supports floating point operations in kernel space.
- Understand OpenMP tasking overheads in order to identify time spent in context switches.
- Develop mktrace a system call delegation tool to offload selective system calls to a kernel thread to emulate multi kernel environments (system call delegation) which is very similar to a rootkit which performs system call hijacking.
- Built a memory dump tool in Linux for malware analysis using ptrace.
- Helped in building a qemu prototype device to evaluate benefits of computation offloading.

Intel **Oregon, USA**

Software Security Research Intern *May 2021 - August 2021*

- Develop supply chain post exploitation payloads (similar to SolarWinds), investigate zero day exploits, both using custom payload and metasploit framework to evaluate Intel anomaly behaviour detection model.

VMware **California, USA**

Summer Intern *May 2020 - August 2020*

- Investigate sources of Jitter in ESXi 7 hypervisor and eliminate them. To understand the sources of Jitter, a detailed analysis of the guest/host software stacks was performed with the help of VPROBES (similar to DTRACE) for collecting fine grained traces from VMM/VMK/Guest worlds and also BPFTRACE/PERF for guest OS analysis.

NexLP **Chicago, USA**

Software Intern *June 2018 – August 2018*

- Worked on multiple projects such as extending Apache Tika (content detection and analysis framework) for advanced data extraction features from documents, OCR Extraction from documents in Java, C#.

Covenant IT Solutions Private Limited **Coimbatore, India**

Software Developer *May 2016 – July 2017*

- Helped in building the vendor, payment and shipping modules for the e-commerce application.
- Played a lead role in migration of e-commerce applications to cloud, hosting and configuring continuous toolchain integration for robust web application development using DevOps framework provided by IBM Bluemix.

Covenant IT Solutions **Coimbatore, India**
Software Engineer Intern *June 2015 – July 2016*

- Integrated e-commerce application with the payment gateway API provided by PAYU for capturing customer payments.

PUBLICATIONS

- ASPLOS 2024
  - **B. Tauro**, Brian Suchy, Simone Campanoni, Peter Dinda, and K.C. Hale. TrackFM: Far-out Compiler Support for a Far Memory World. *Proceedings of the 29th ACM International Conference on Architectural Support for Programming Languages and Operating Systems*.
- TPDS 2021
  - **B. Tauro**, C. Liu, and K.C. Hale. Modeling Speedup in Multi-OS Environments on real world multi-kernels. *IEEE Transactions on Parallel and Distributed Systems*, September, 2021.
- MASCOTS 2019
  - **B. Tauro**, C. Liu, and K.C. Hale. Modeling Speedup in Multi-OS Environments. *Proceedings of the 27th IEEE International Symposium on the Modeling, Analysis and Simulation of Computer and Telecommunication Systems*, October, 2019.

POSTERS

- GCASR 2019
  - **B. Tauro**, C. Liu, and K.C. Hale. Modeling Speedup in Multi-OS environments. Poster at the 8th Annual Greater Chicago Area Systems Research Workshop, May, 2019.
- Chameleon User Meeting 2019
  - Infiniband HPC RDMA Aware Drivers for light-weight Kernels, Presentation at the Chameleon User Meeting at University of Texas Austin, February, 2019.

CURRENT PROJECTS

1. Compiler Assisted Remote Memory

- Current software based far-memory solutions, have been able to improve memory utilization in cloud data centers, by enabling applications with high memory demands to be met by utilizing memory from a remote server with fast network operations. However, the existing approaches have been unable to strike the right balance between performance and transparency provided to applications. In this project, we show how compiler aided kernel based far memory solution can strike the right balance between transparency and performance by using modern day compiler frameworks.
- This project is part of the Interweaving Project, a collaborative effort with Northwestern University to redesign the parallel hardware/software Stack.
  - http://interweaving.org

2. Modeling application speedup in multi OS environments
   - With hardware silicon reaching its limits, there has been significant research in OS kernels, currently there is empirical study on application performance in multi-kernels (Intel mOS, IHK/McKernel) but there has not been a theoretical study on application speedup in multi-kernel environments, our group is the first to model application speedup in multi-kernels and provide insight to the developer on whether an application can benefit from running on a multi-kernel environment such as Intel mOS. I used strace to capture the system call traces of the application and mktrace a tool developed at HExSA Lab for simulating application performance on multi-kernel environments. Our model can determine the application speedup on a multi-kernel without having to run the application on a multi-kernel.
3. Dynamic behavior analysis of malwares using memory dumps
   - Current malware analysis tools rely on the underlying operating system for detecting systems infected with malwares, which make them less effective when there are major updates in the operating system, so in order to avoid having to change malware tools for every update of the operating system, we focus on the behavior of malwares, specifically how does the state of the memory change during an attack and we intend to build a tool for detecting malwares without having to make any assumptions of the underlying operating system on which the application runs on and also without compromising the performance of the kernel.

COURSE PROJECTS

- Independent Study (CS597 - IIT)
  - Built an operating system from scratch with memory management unit, process subsystem, interrupt handling, serial port communication (UART), exception handling for a cortex 53 quad core processor (Raspberry Pi 3).
- Compiler Construction (COMP_SCI 322 - Northwestern University)

- Developed a new control flow programming language from scratch for the x86 architecture where the back-end of my compiler closely resembles modern day compilers such as LLVM including features such as advanced graph coloring, instruction selection using maximal munch, control flow graphs, CISC instructions and my programming language included support for advanced data structures like Tuples, Tensors.

- Code Analysis and Transformation (COMP_SCI 323 - Northwestern University)
  - Perform Constant Propagation, Constant Folding which included alias analysis, inter procedural analysis and loop transformations using LLVM over a domain specific language.
- Data Intensive Computing (CS554 - IIT)
  - Helped in porting XTASK (eXTreme fine-grAined concurrent taSK invocation runtime) into Nautilus (aerokernel) for scheduling billions of tasks with very low latency and high throughput for applications running in kernel space.
- Design and Analysis of Operating Systems (CS551 - IIT)
  - Built a pseudo device driver for the Minix operating system for analysis of blocked and asynchronous IO.
  - Built an inter process messaging service similar to JMS in Minix using Minix IPC with deadlock avoidance and recovery mechanisms (Producer Consumer model).
- Virtual Machines (CS595 - IIT)
  - Developed a MOS 6502 emulator and a custom JVM with (mark and sweep) garbage collector based on the Oracle JVM specification.
- Advanced Operating Systems (CS550 - IIT)
  - Built distributed file sharing systems such as the Napster and Gnutella-style P2P, with data consistency mechanisms (push and pull based approach).
- Parallel and Distributed Systems (CS546 - IIT)
  - Developed and evaluated Conway's game of life performance on GPU using CUDA, 2D convolution with SPMD and task/data parallel techniques using MPI.
- Cloud Computing (CS553 - IIT)
  - Developed an custom external tera sort algorithm with comparative performance analysis on Apache Hadoop and Spark.
- Artificial Intelligence (CS480 - IIT)
  - Implemented Alpha-beta pruning, simple decision making, and several search algorithms in Python.

BLOGS

- Exploring Custom InfiniBand Drivers for Specialized OS Kernels, April 2019.
  - https://www.chameleoncloud.org/blog/2019/04/19/exploring-custom-infiniband-drivers-specialized-os-kernels/

AWARDS/EXTRA-CURRICULAR

- Vice president of UPE (Upsilon Pi Epsilon) International Honors Society for Computing and Information Disciplines at IIT Chicago.
- First place in Code A-Thon (hacking competition) at Mindkraft 2016 (national event) held at Karunya University.
- Second place in Help Dexter Code (hacking competition) at Mindkraft 2015 (national event) held at Karunya University.
- Active reviewer and member of Stack Overflow community (briantaurostack7).

CERTIFICATIONS

- IBM badge for completion of cloud developer connect session on serverless computing, cloud security and performance, containers, server less programming and API connect.
- IT foundation skills assessment by Cognizant.
- Competed grade 5 in violin from Trinity College of London.

GROUP AFFILIATIONS

- HExSA Lab
- Scalable Computing Software Laboratory (SCS)
- Northwestern Parallelism Group

TECHNICAL SKILLS

Programming Languages: C, LLVM, C++, Java, C#, Assembly, Shell, Python
Parallel Programming: MPI, CUDA, OpenMP, Pthreads
Benchmarking Softwares : HPL, pmbw, IOzone, Iperf, SPEC CPU 2017, NAS
Operating Systems: Linux, Macintosh, Windows, Minix, mOS, IHK/McKernel, Nautilus
Cloud Environments: AWS, IBM BLUEMIX, Chameleon
Databases: Oracle, Dash, MySQL, Mongo

Virtual Environments: kvm, qemu, VMware, VirtualBox, ESXi
Tracing Tools: strace, systemtap, eBPF, vprobes, perf
Miscellaneous Softwares: LaTeX, Packet Tracer, Wireshark, GDB, PXE, iDRAC